

F-1 G. 1

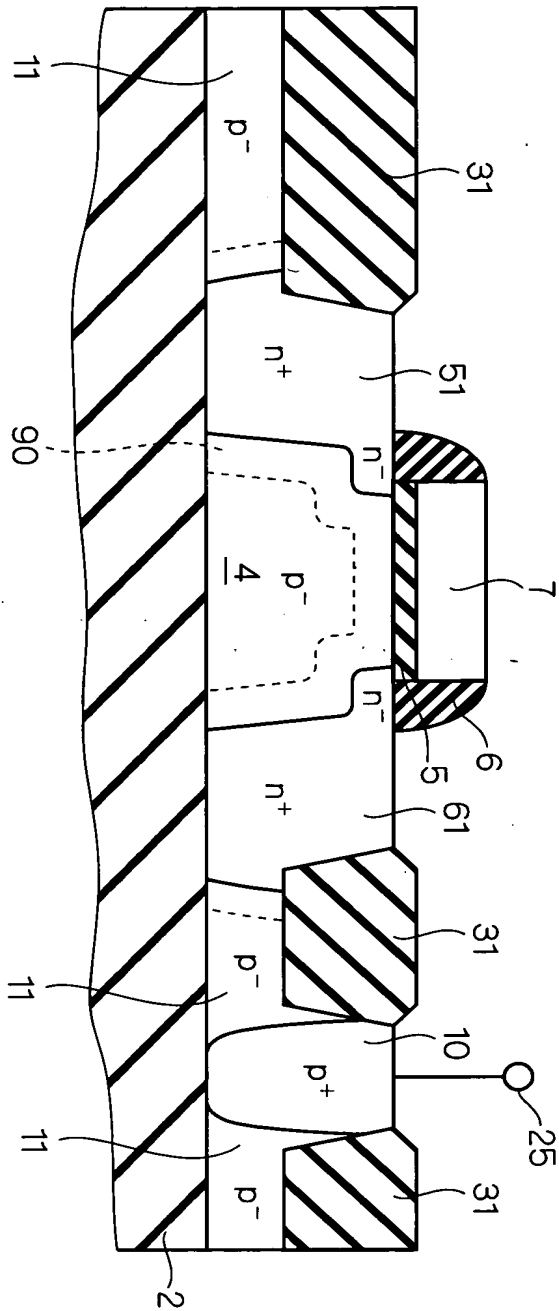


FIG. 2

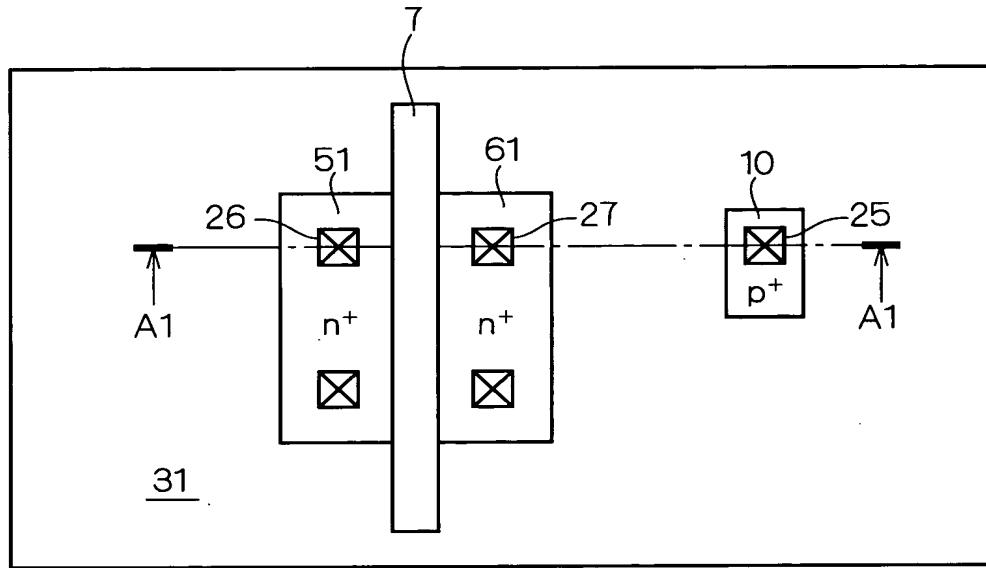
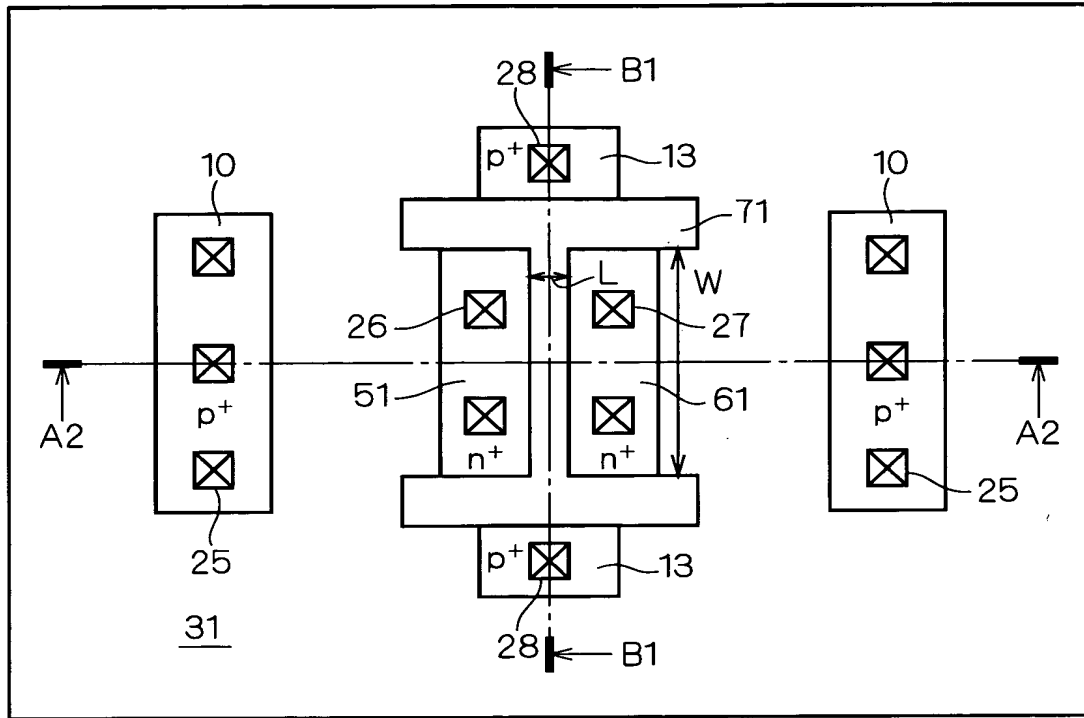


FIG. 2

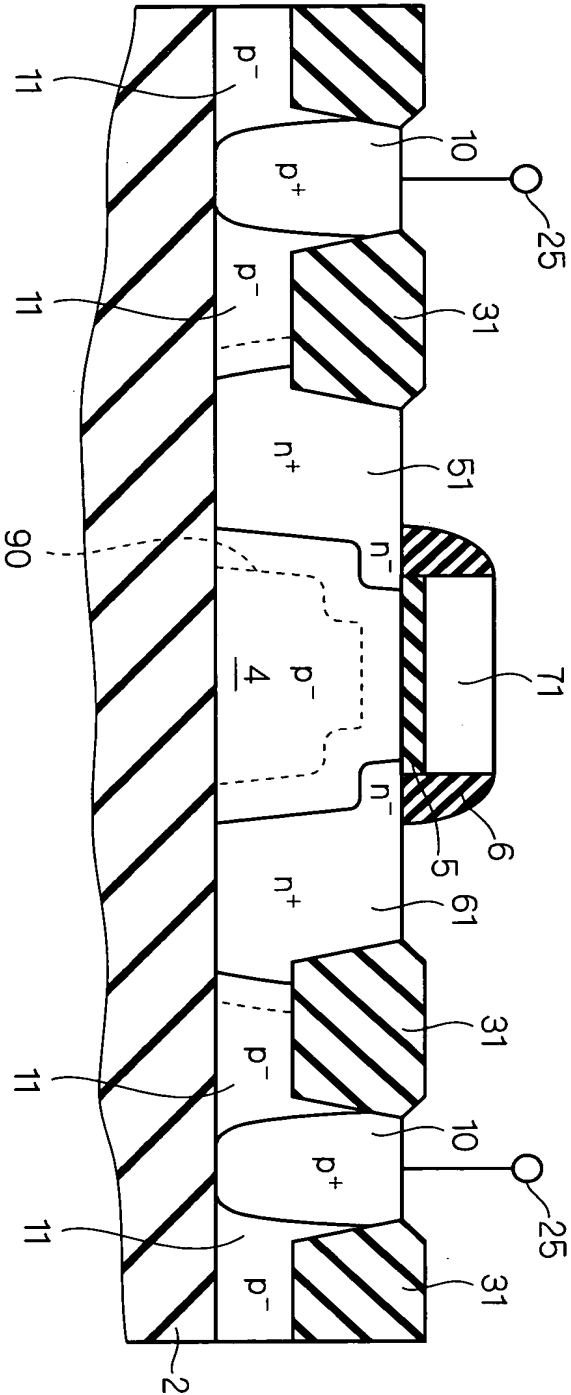
FIG. 3



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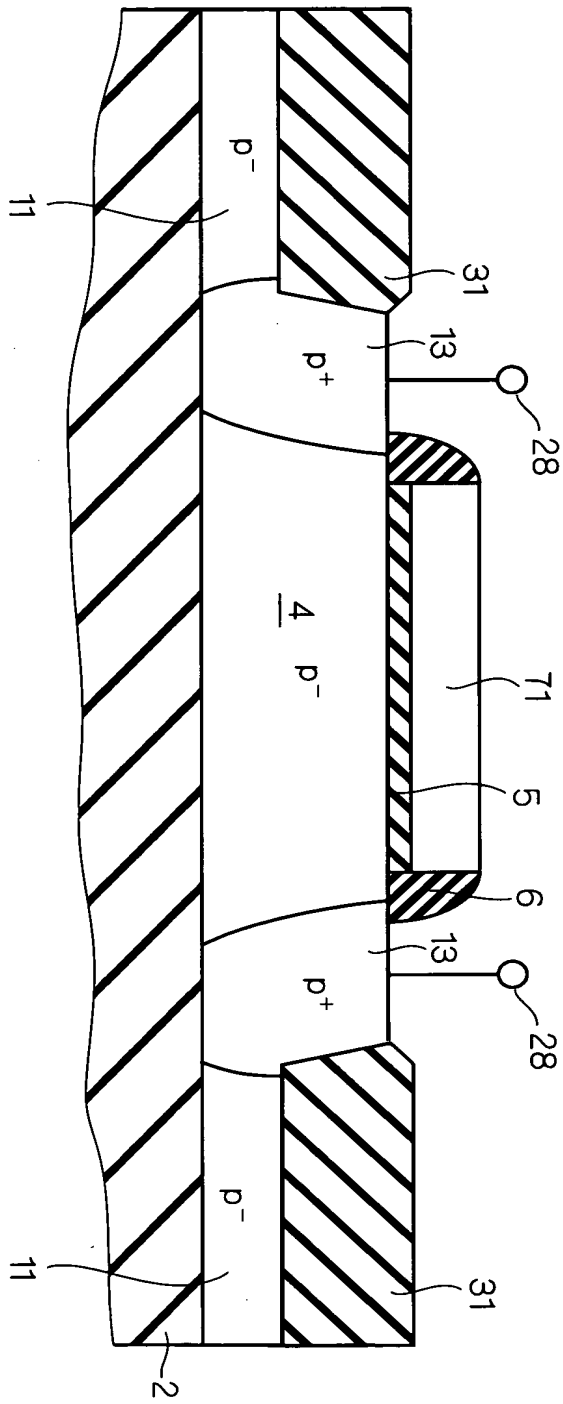
104011-10098860

FIG. 4



102017-40098660

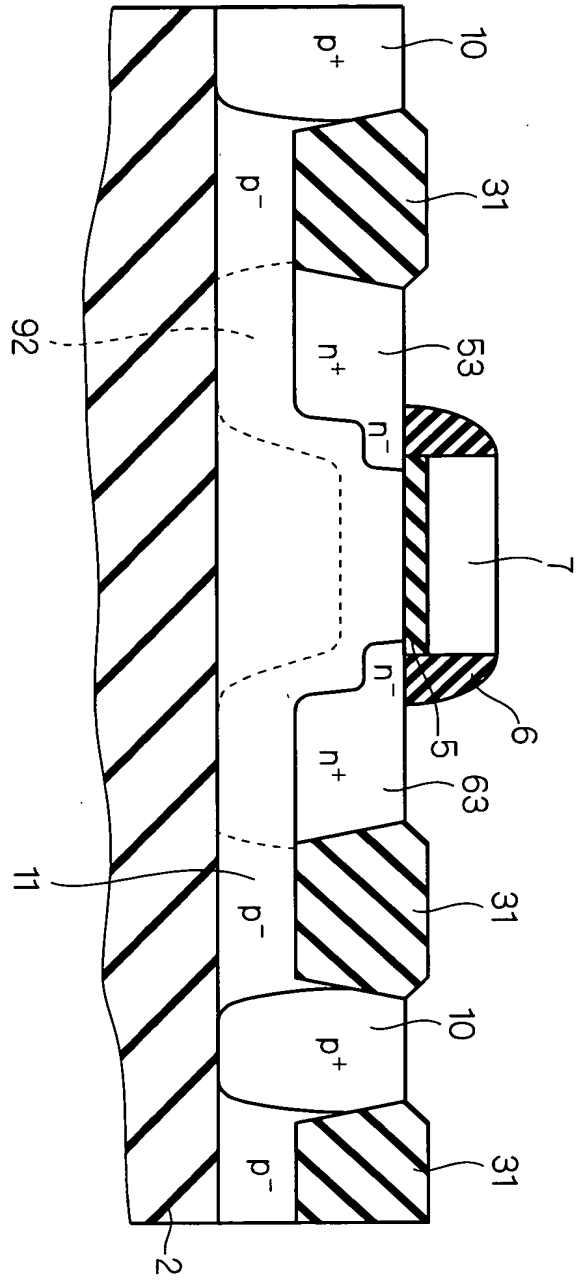
FIG. 5





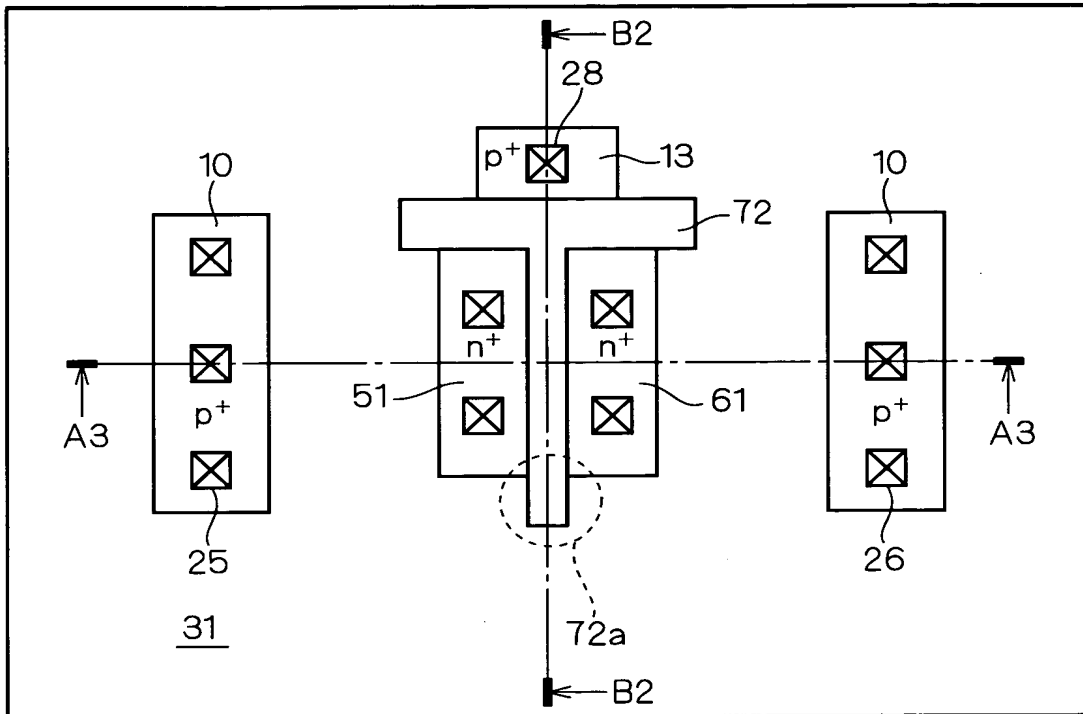
104011-10098660

FIG. 7



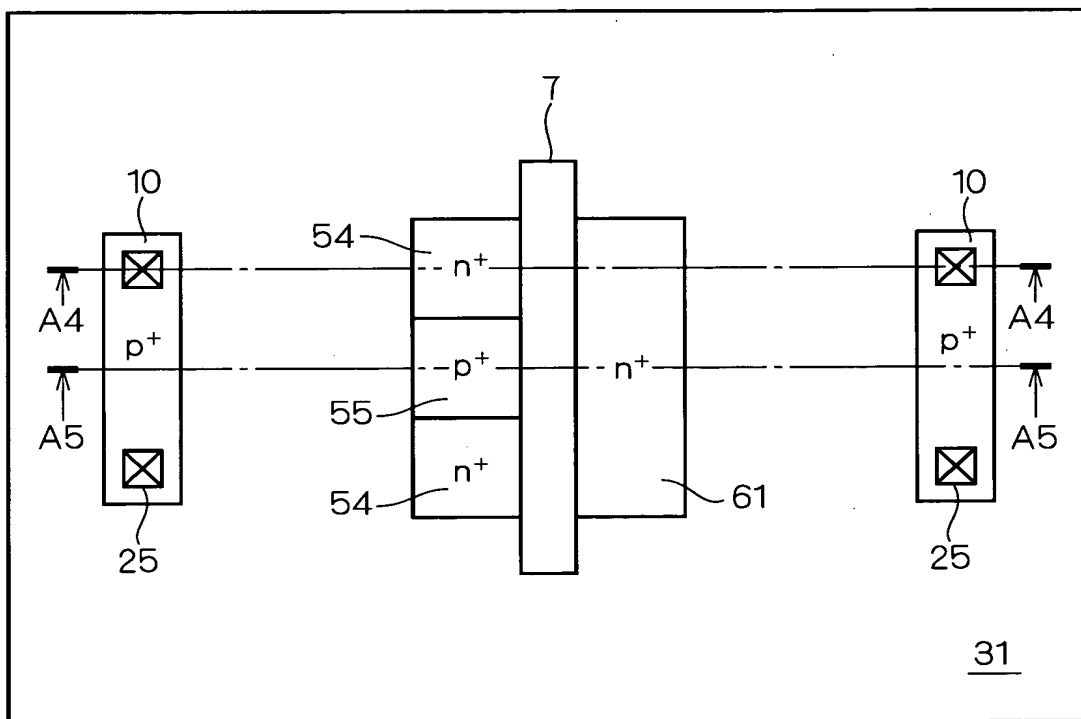
[illegible]

FIG. 9



09986004-110701

FIG. 10

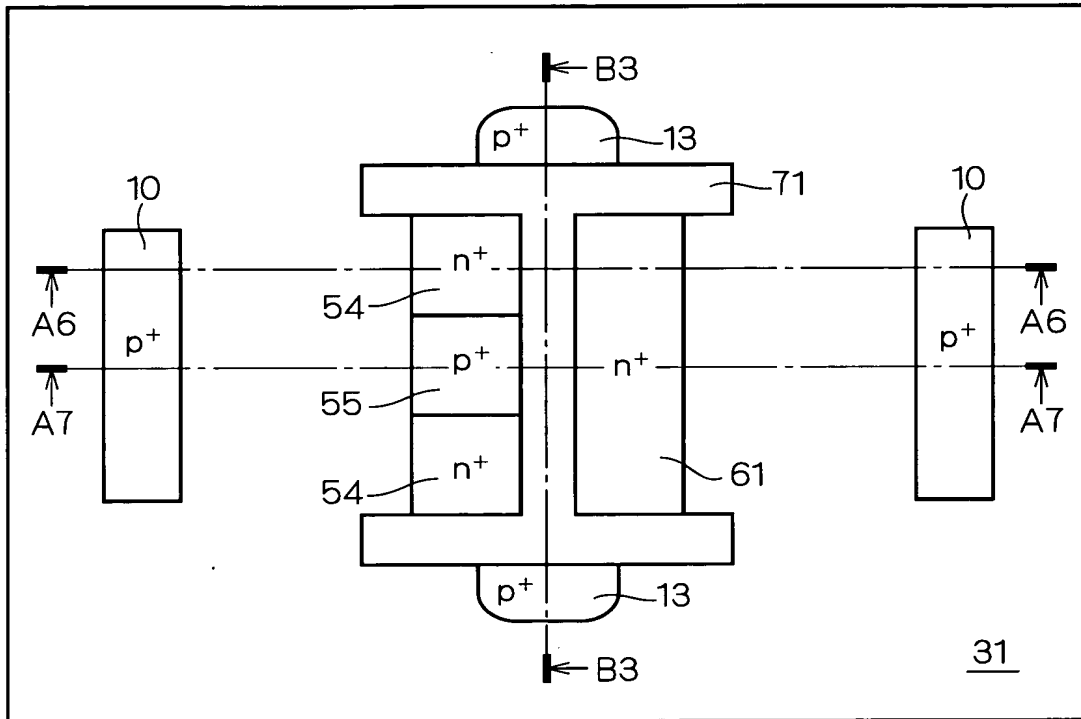


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[illegible]

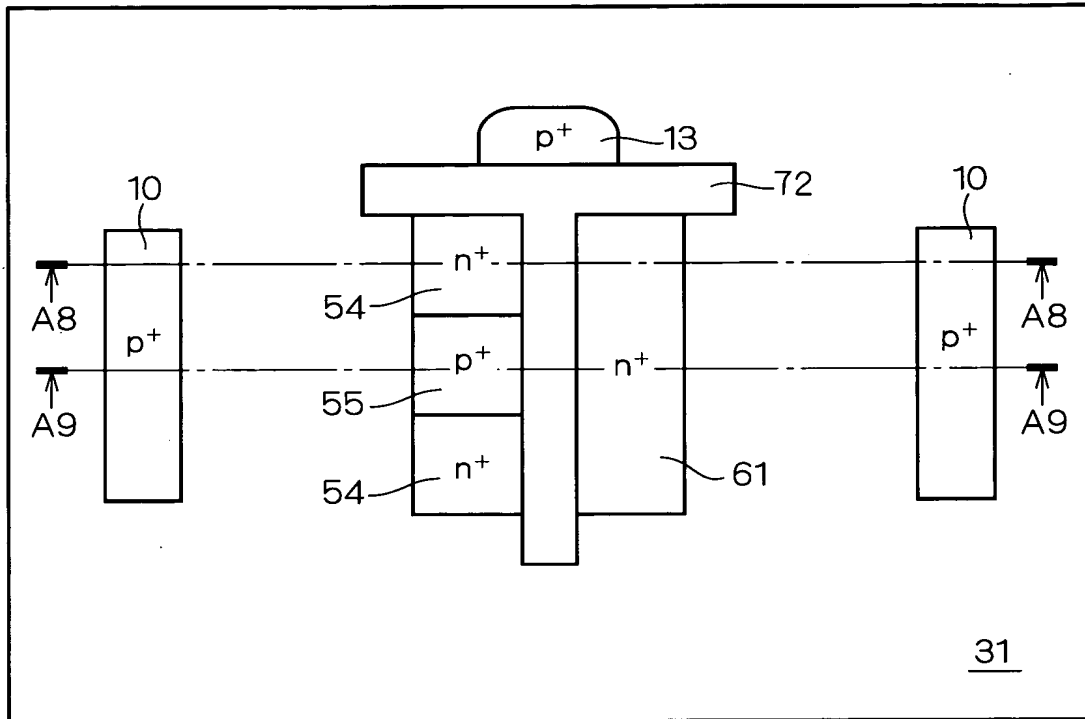
This diagram shows a cross-sectional view of a semiconductor device. It features a central U-shaped structure (7) with a bottom layer (6) and a top layer (5). The structure is surrounded by a substrate (2) with various doped regions:  $p^+$  (10),  $p^-$  (31),  $n^-$  (4),  $n^+$  (61), and  $p^-$  (11). The device is also labeled with 10, 11, and 2.

FIG. 13



09986004-110701

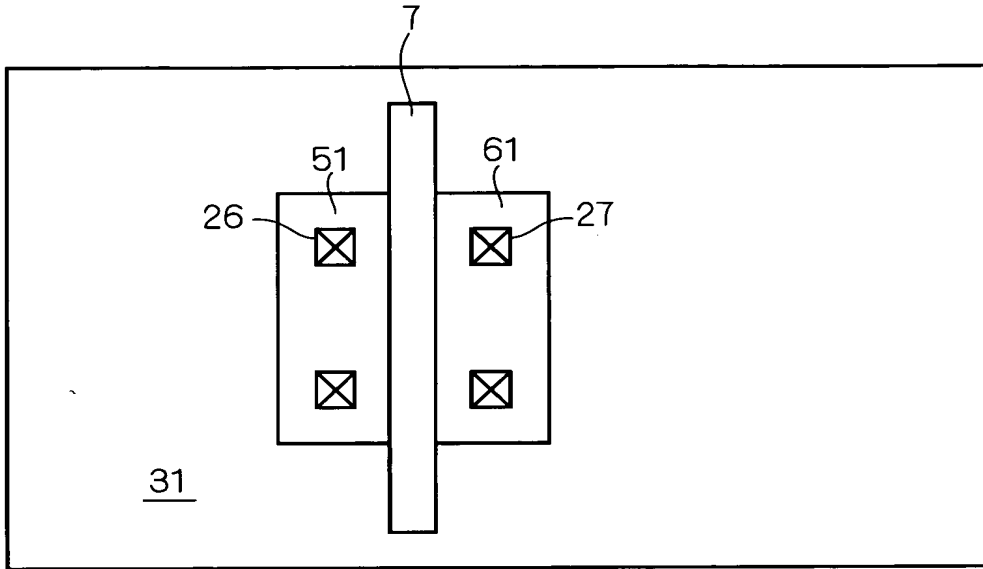
FIG. 14



09986004-110701

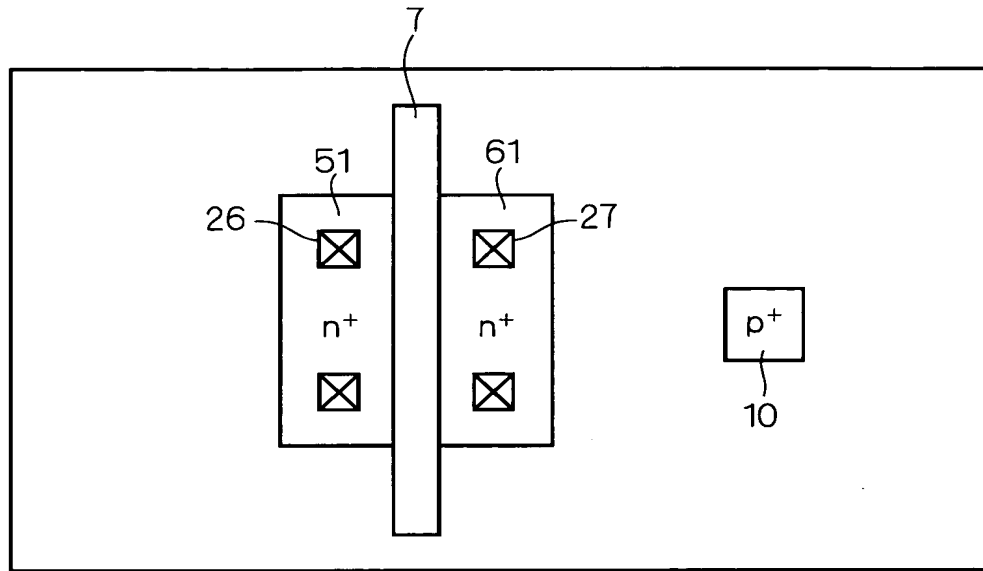


FIG. 16



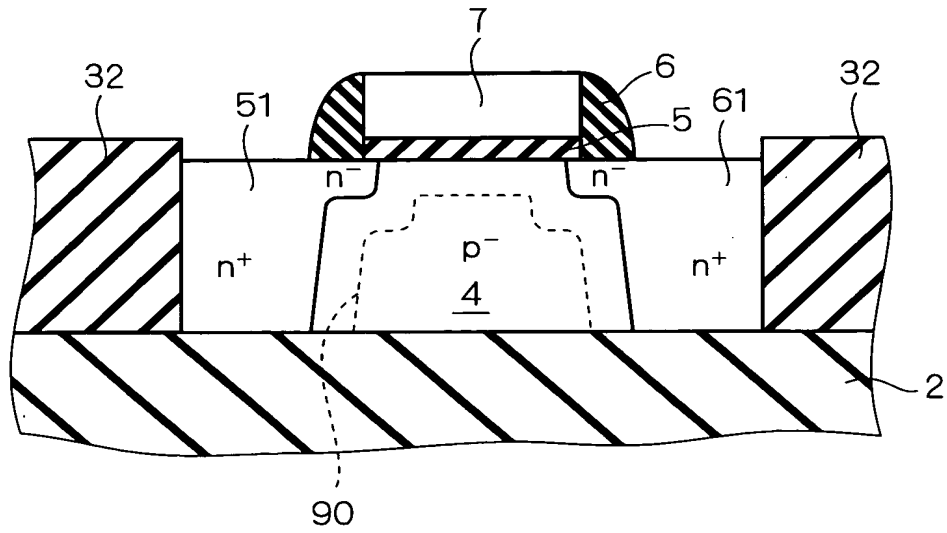
09085004-110701

F I G . 1 7



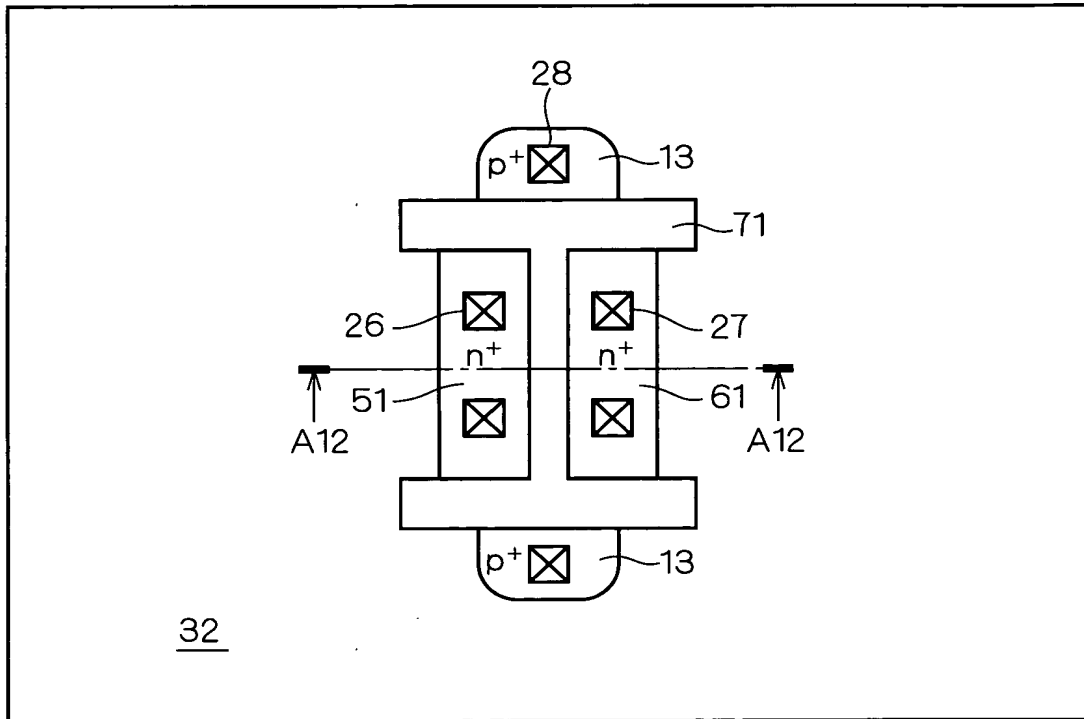
09986004-110701

F I G . 1 8



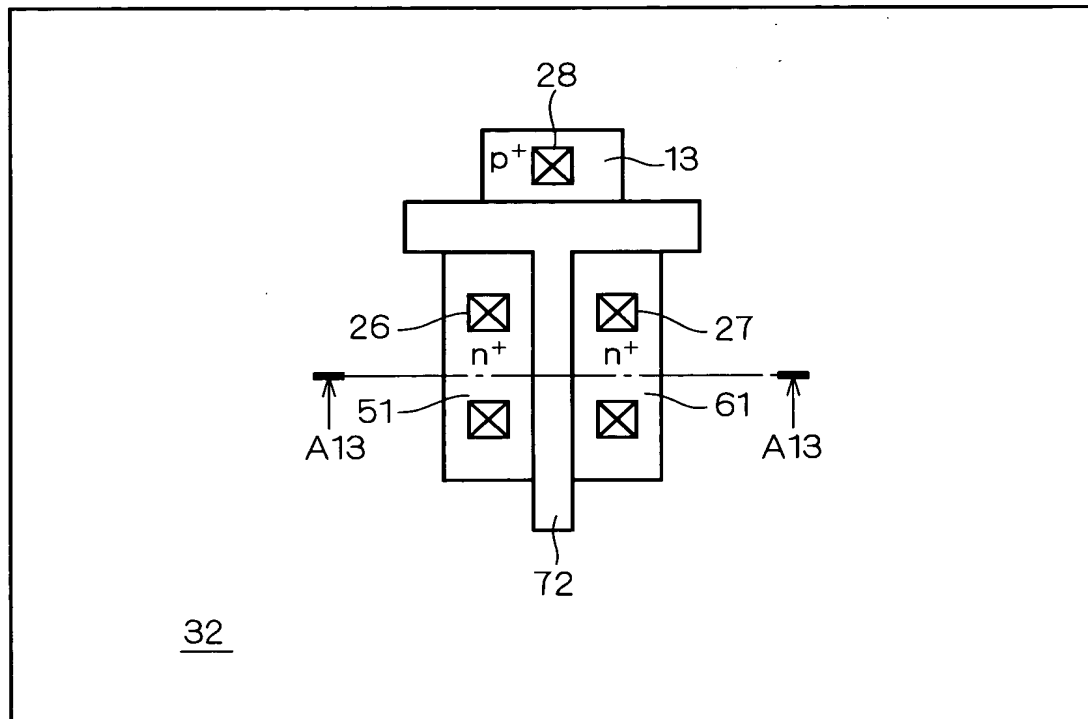
09986004-110701

FIG. 19



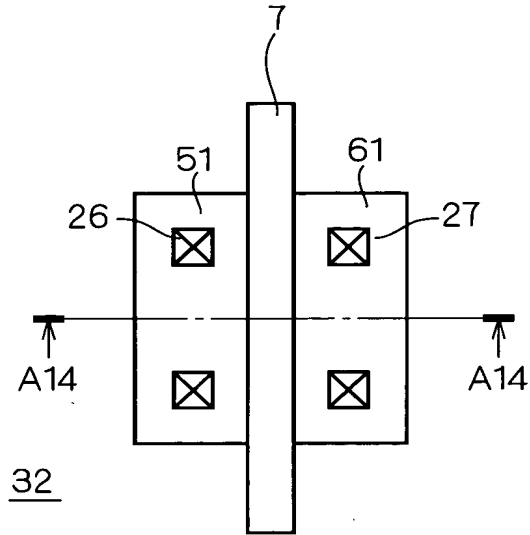
09986004-110701

F I G . 2 0



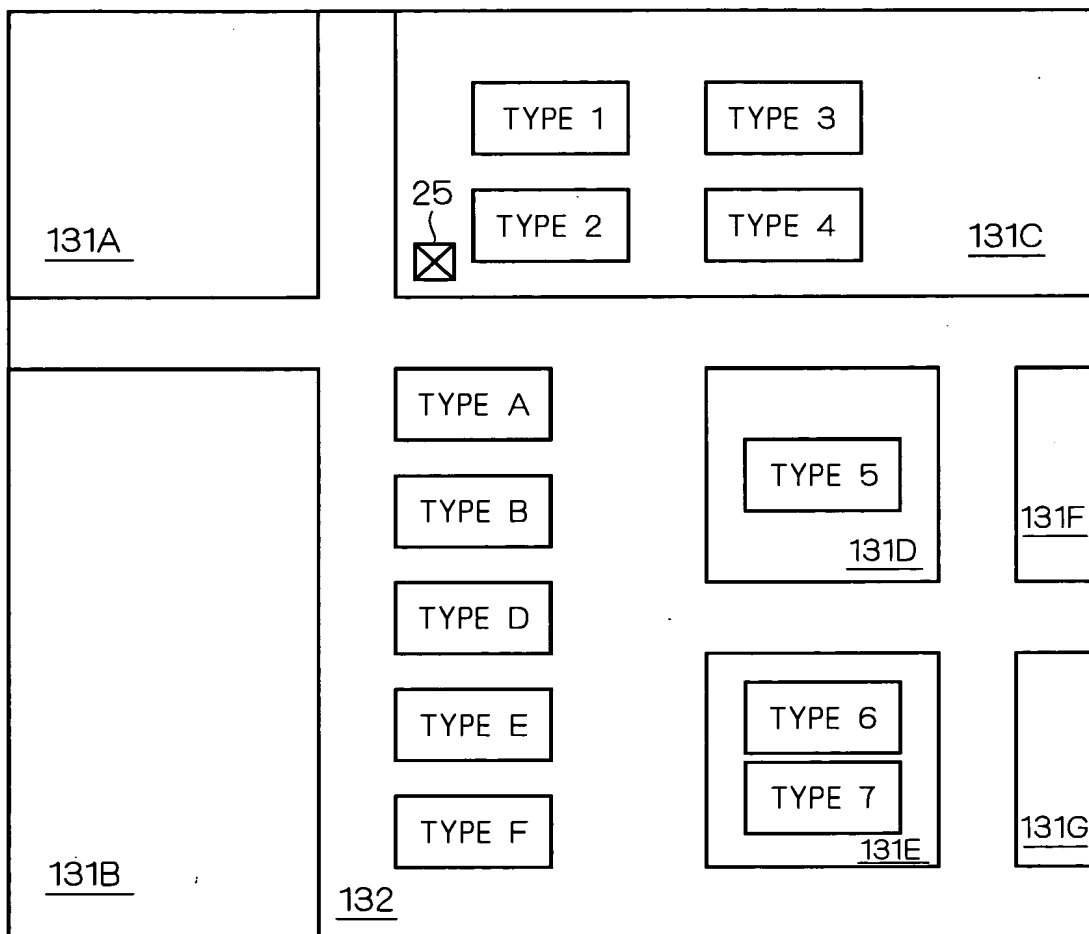
09986004.110701

F I G . 2 1



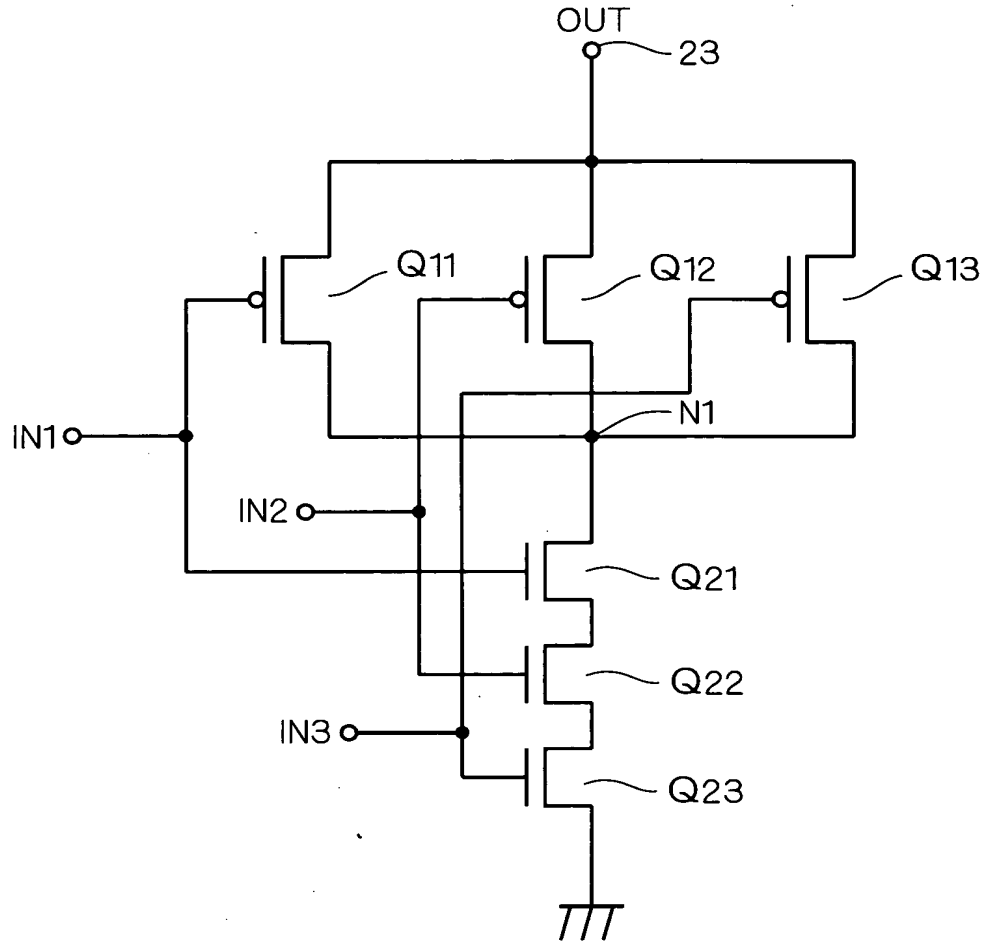
00986004.110701

F I G . 2 2



0986004-110701

FIG. 23



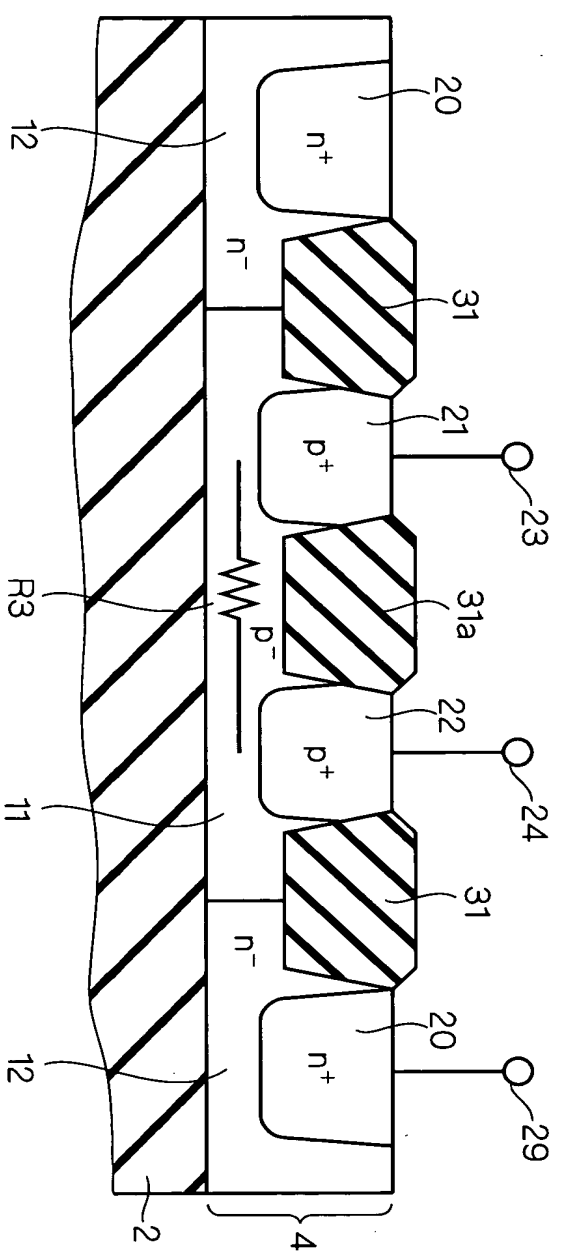
098600410701

The diagram illustrates a 16-bit carry-lookahead adder (CLA) circuit. It consists of a chain of 16 full adders. The first adder has inputs **IN** and **0** (ground), and outputs **S14** and **N2**. The chain is composed of stages labeled **Q14**, **Q15**, and **Q25**, with an output labeled **IV**. The circuit is shown as a repeating structure of three stages, with an ellipsis indicating the continuation of the chain.

[illegible]

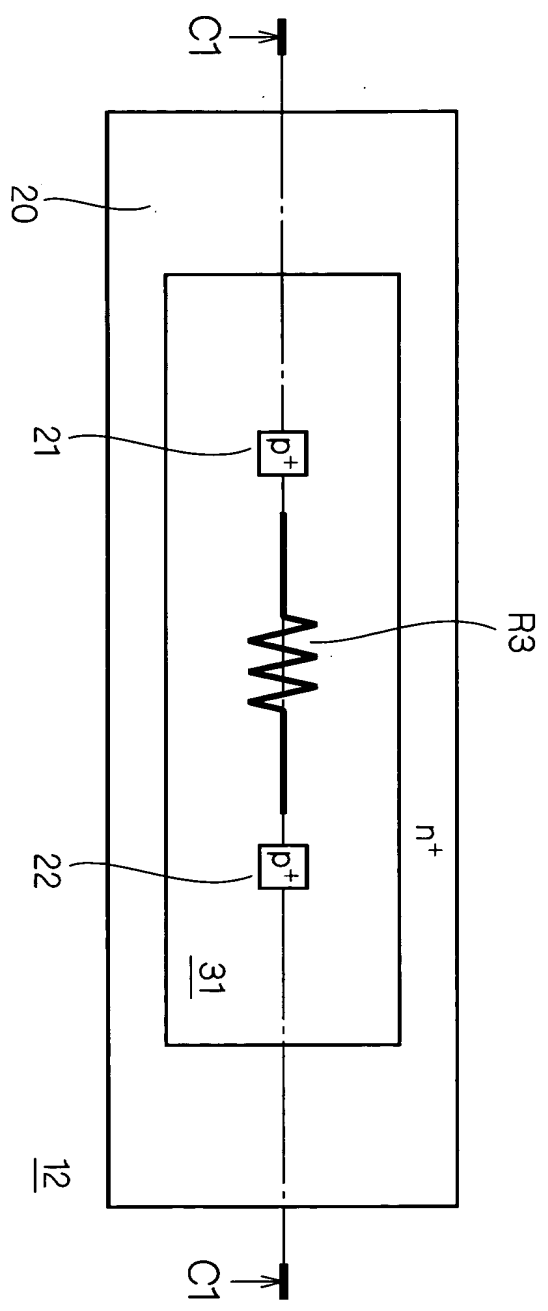
104017-40098660

FIG. 26



104011-40098660

FIG. 27



FOUOIT-10098660

FIG. 28

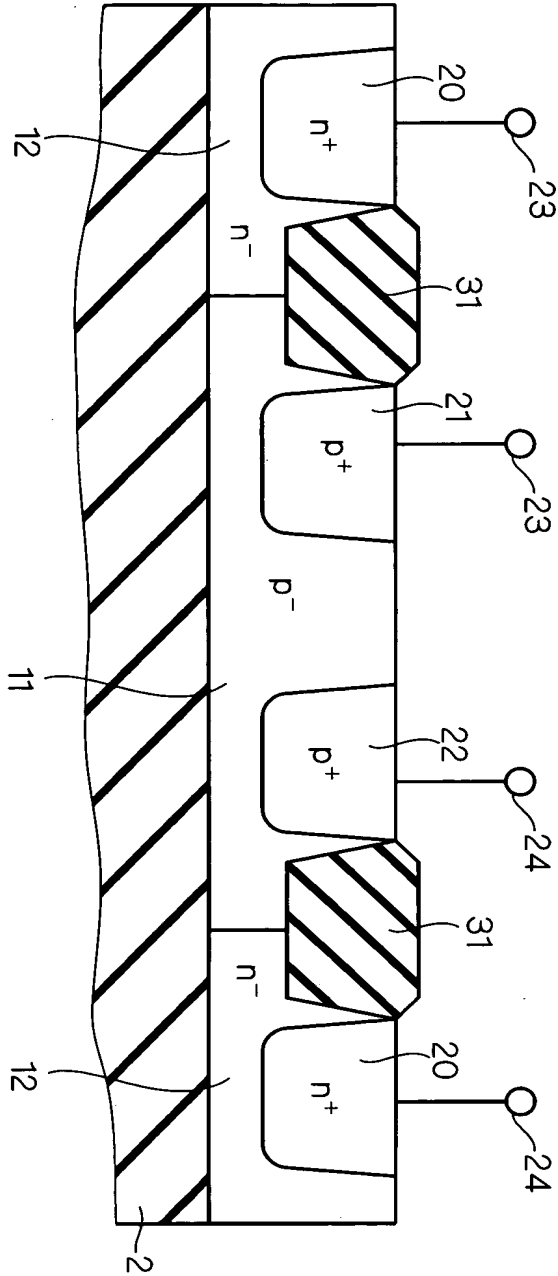


FIG. 29

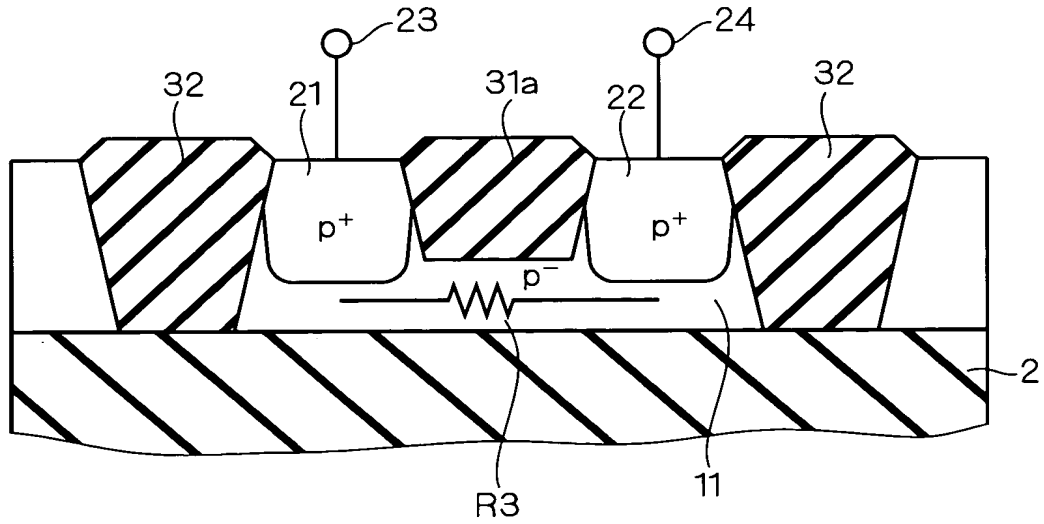


FIG. 29

FOOT-10098650

FIG. 30

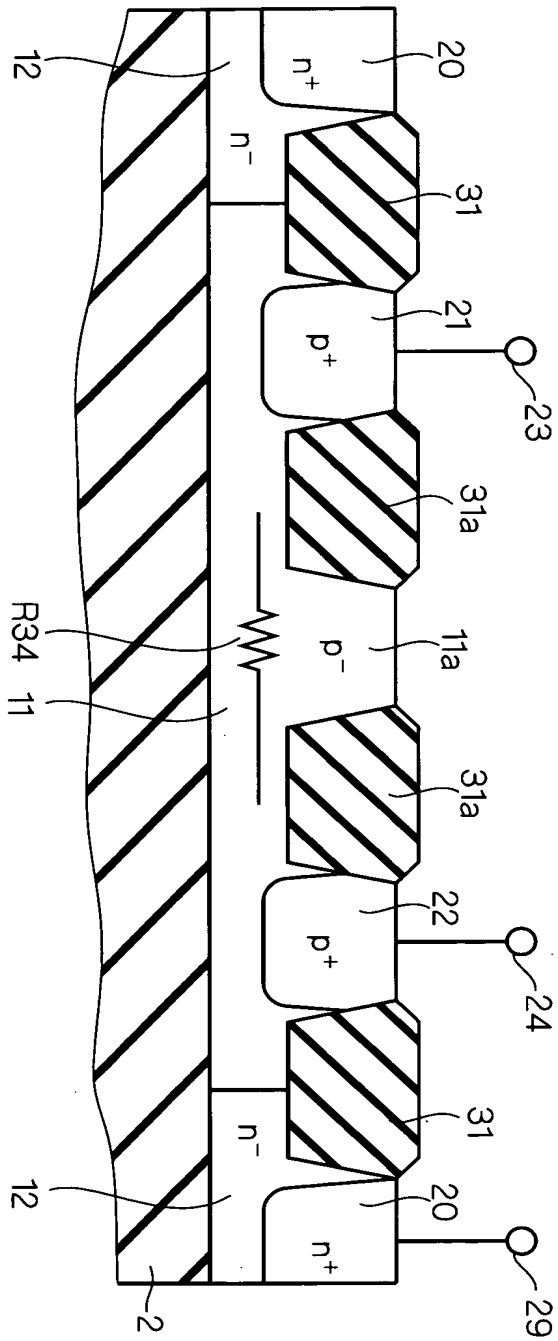
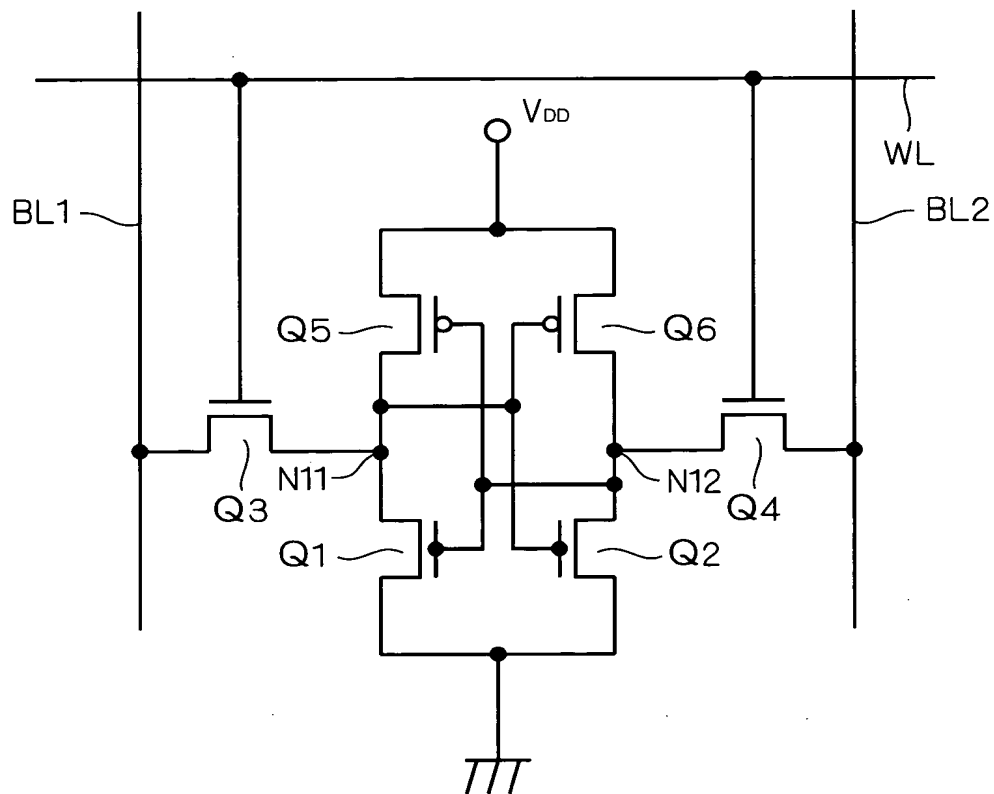


FIG. 31



09986004.110701

FIG. 32

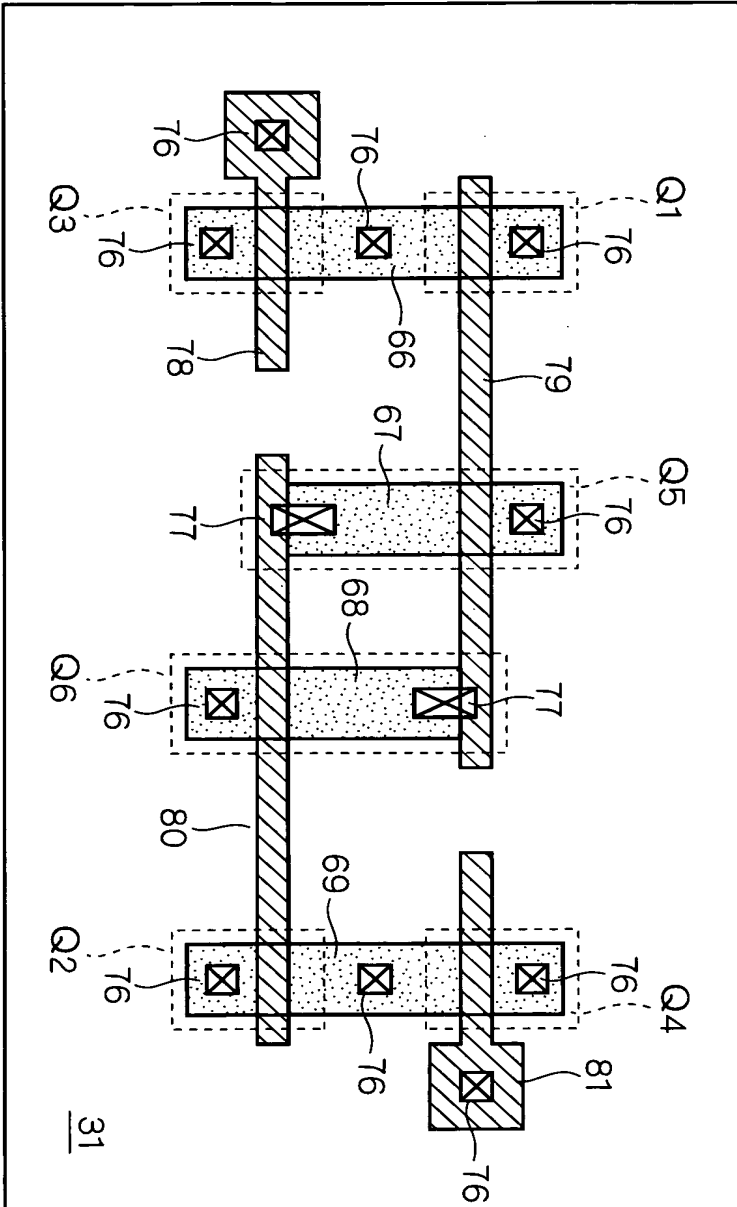


FIG. 33

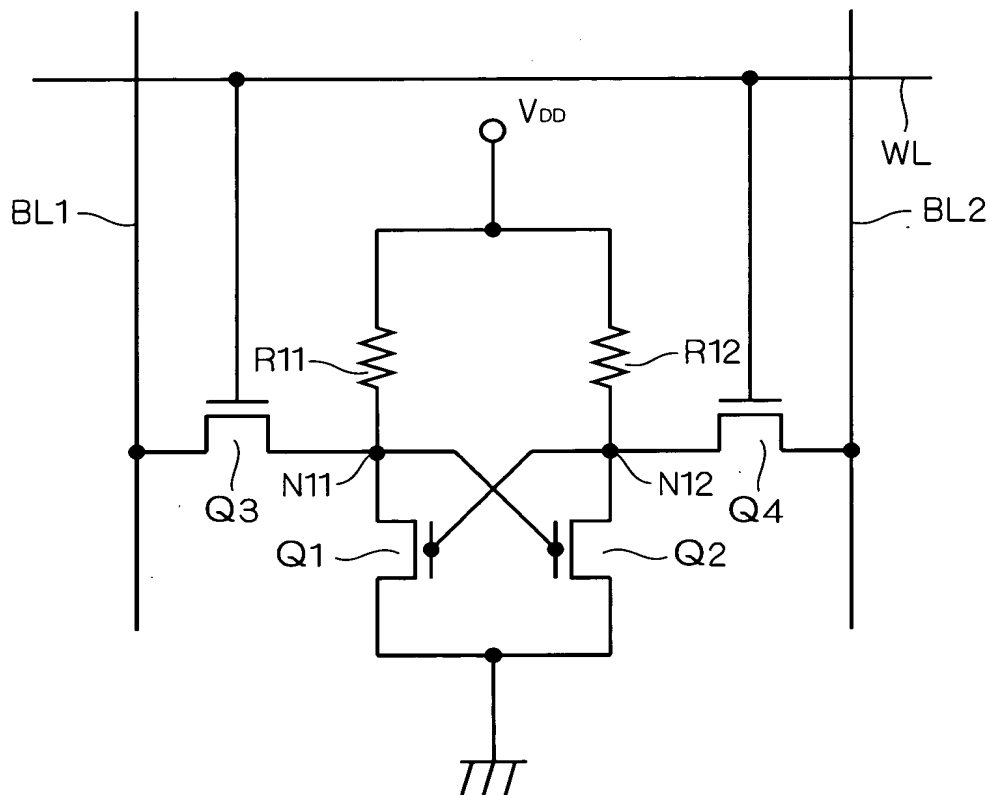


FIG. 33

FIG. 34

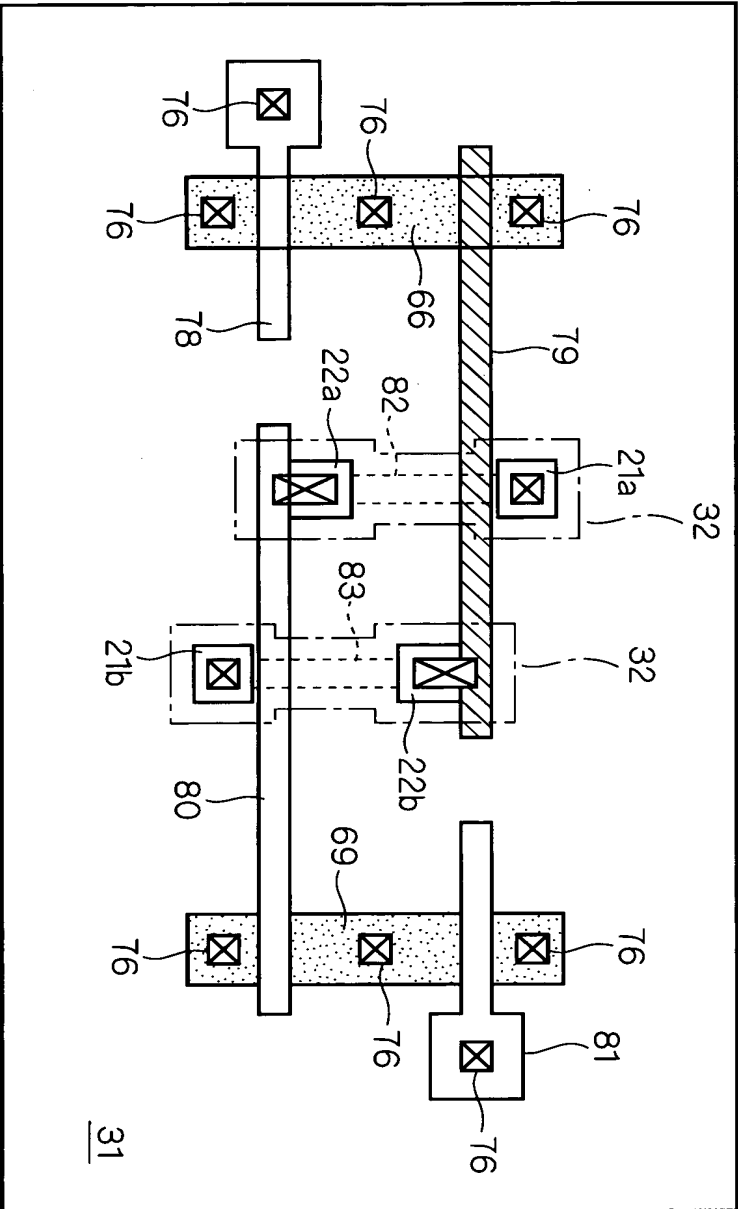


FIG. 36

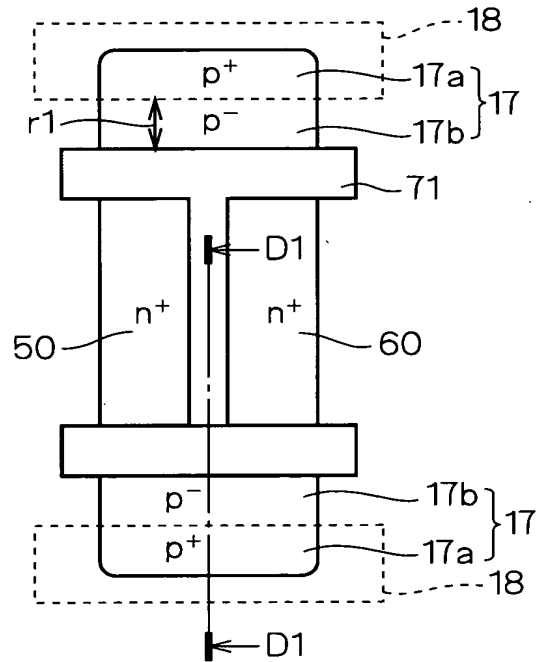
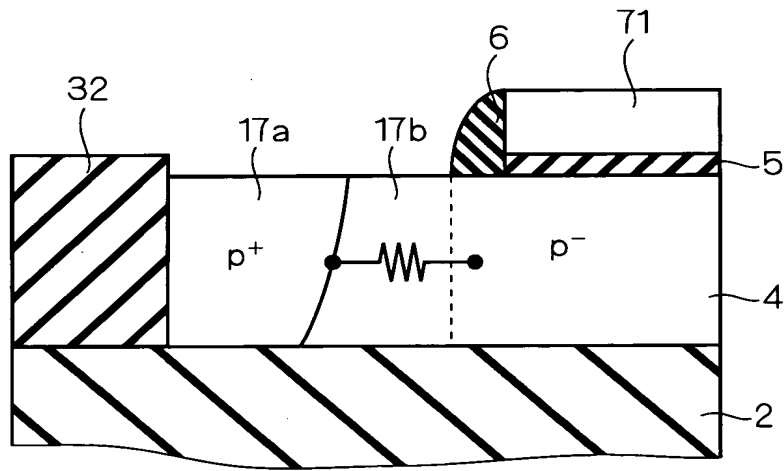


FIG. 37



09986004-110701

FIG. 38

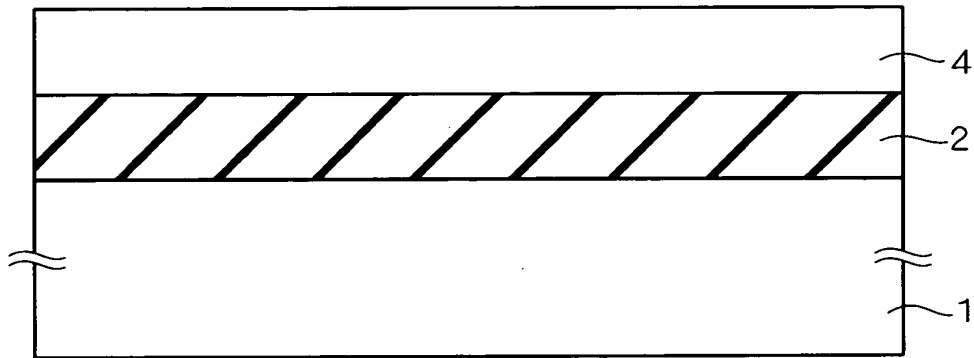
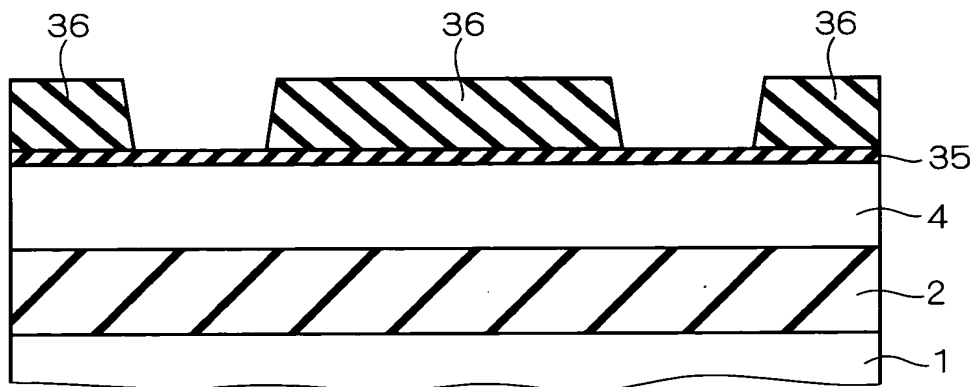


FIG. 39



09986004.110701

FIG. 40

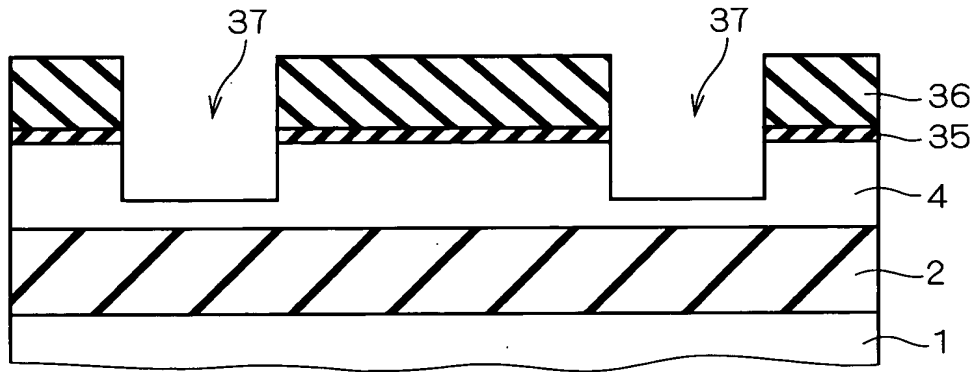
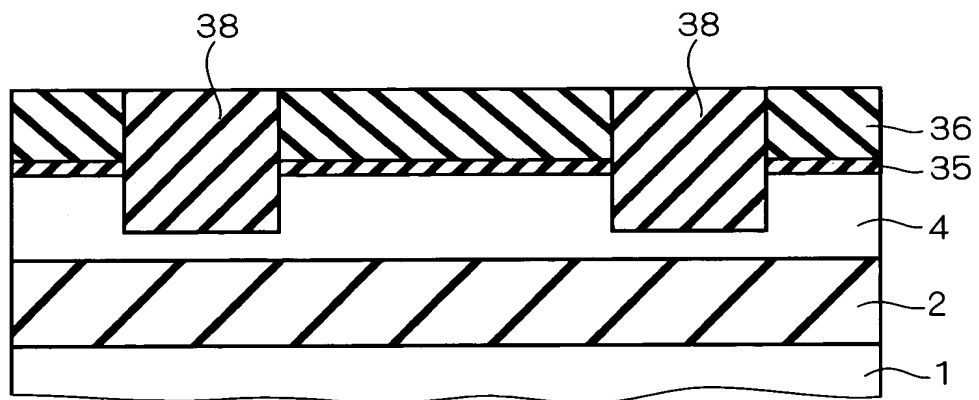
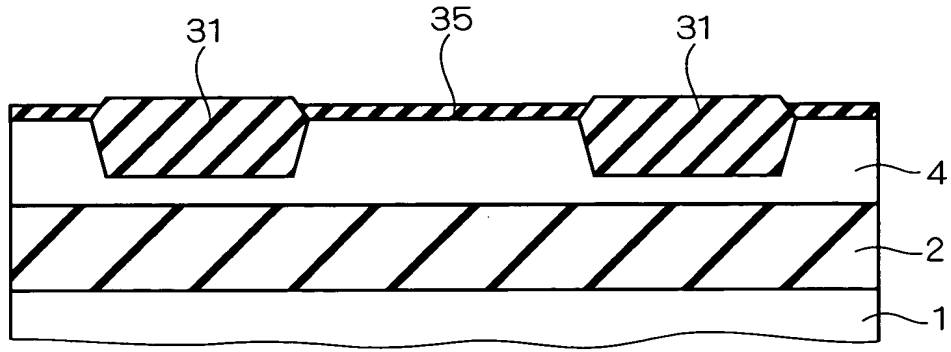


FIG. 41



0986004-110701

FIG. 42



09986004.110701

This diagram shows a cross-sectional view of a semiconductor device. A substrate 1 is shown at the bottom, with a layer 2 on top of it. A patterned layer 31 is formed on layer 2, with a thin layer 40 on top of it. A top layer 11 is shown above the patterned layer 31. Arrows indicate a process flow or pressure application.

104011-40038660

FIG. 44

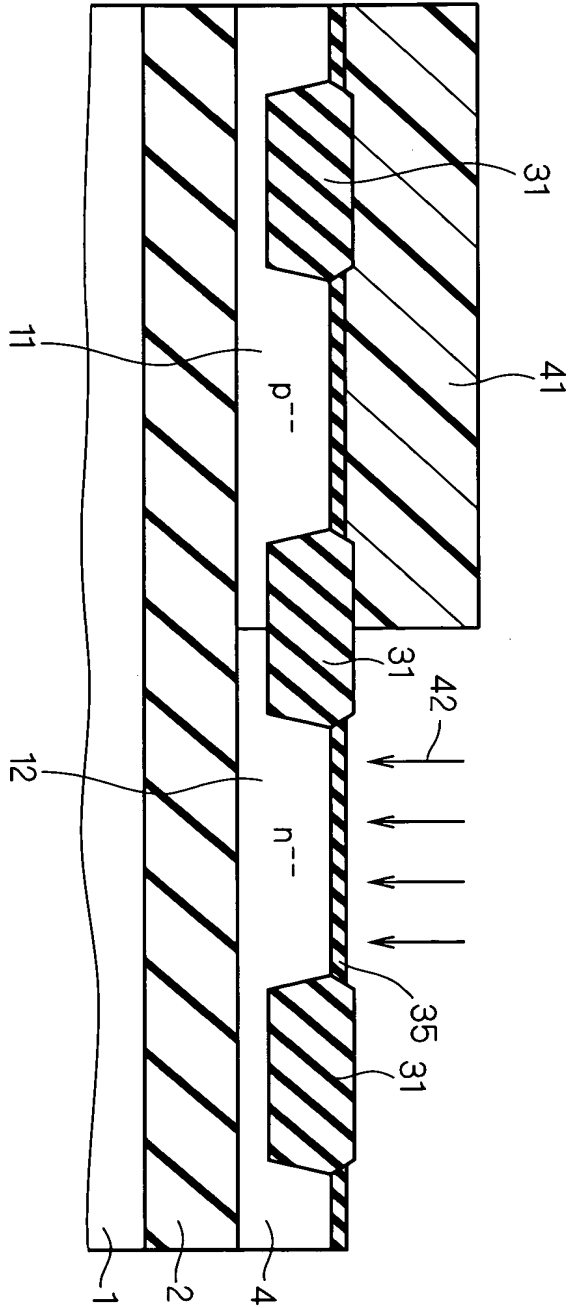
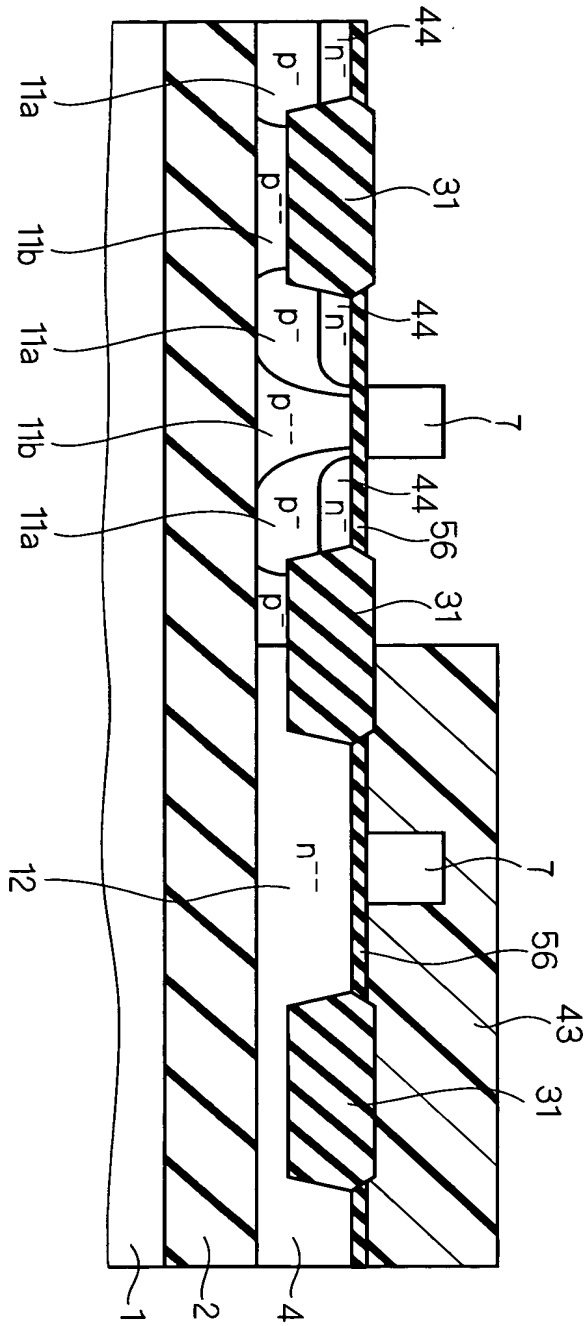




FIG. 46



FOOT-10098660

FIG. 47

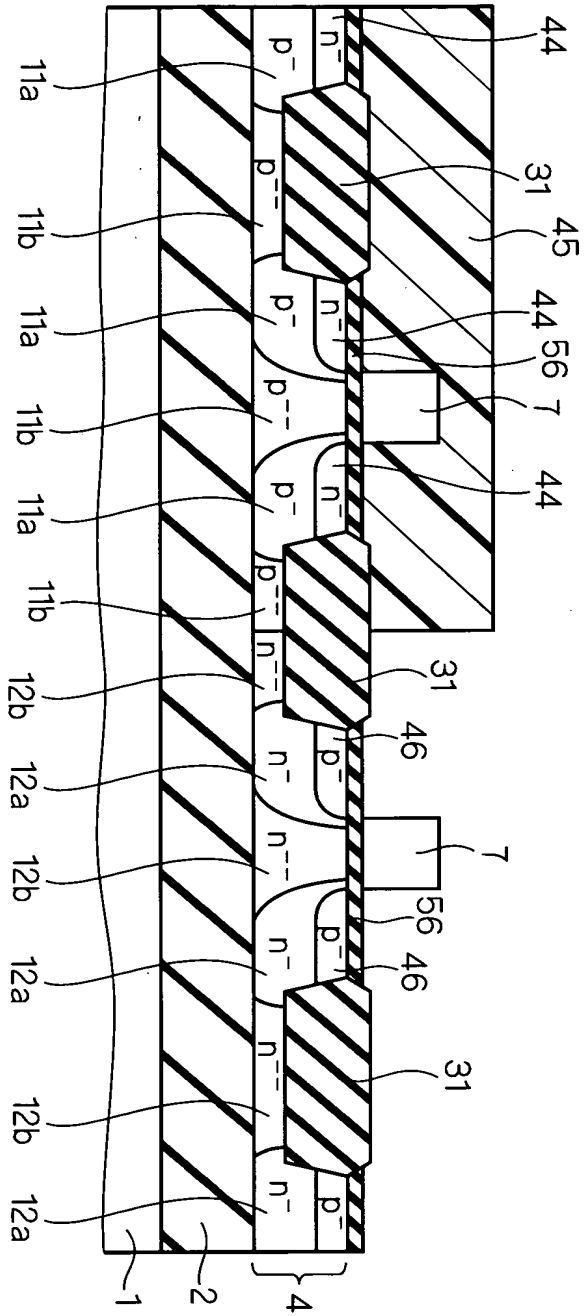


FIG. 48

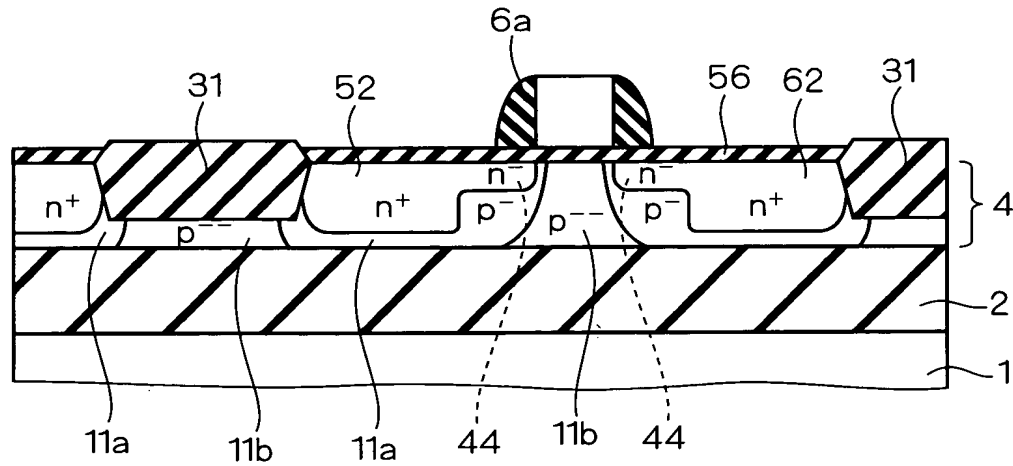
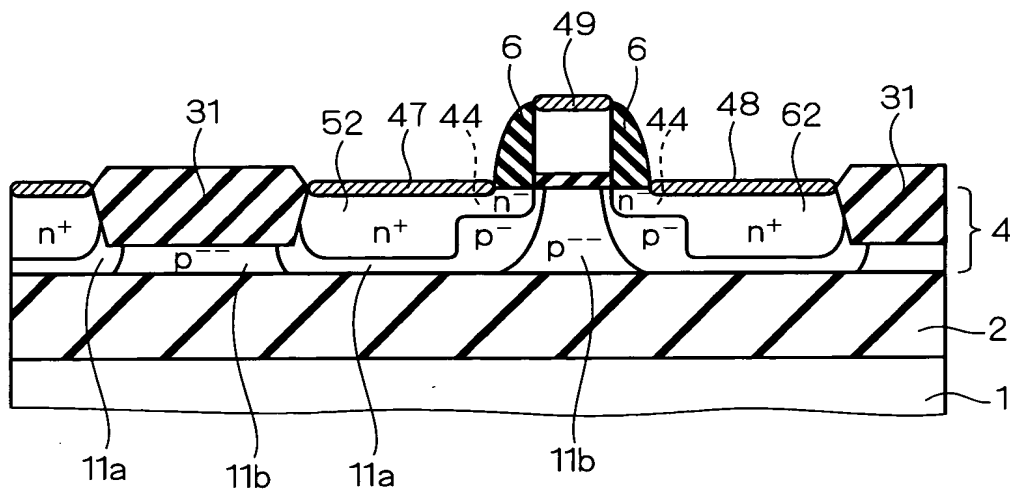


FIG. 49



0995004-110701

FIG. 50

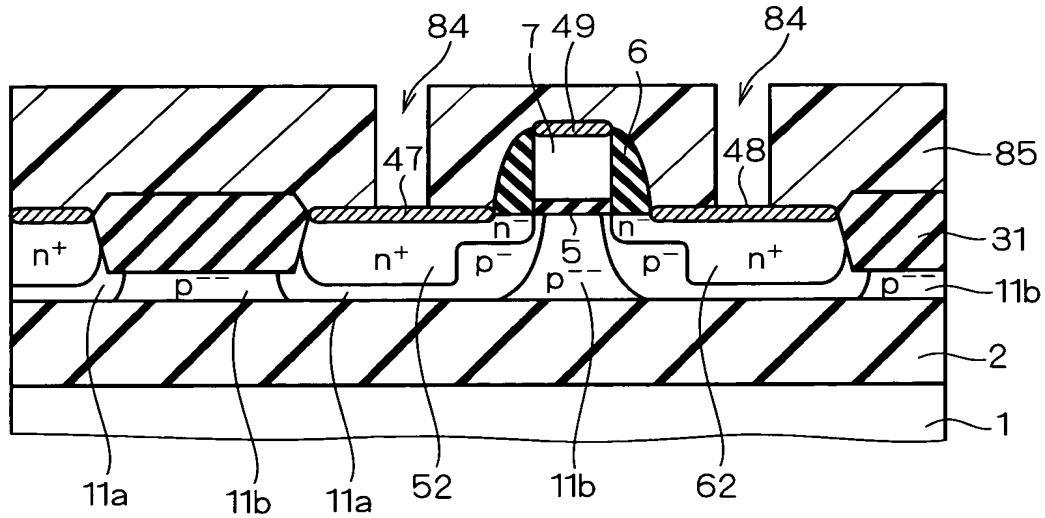
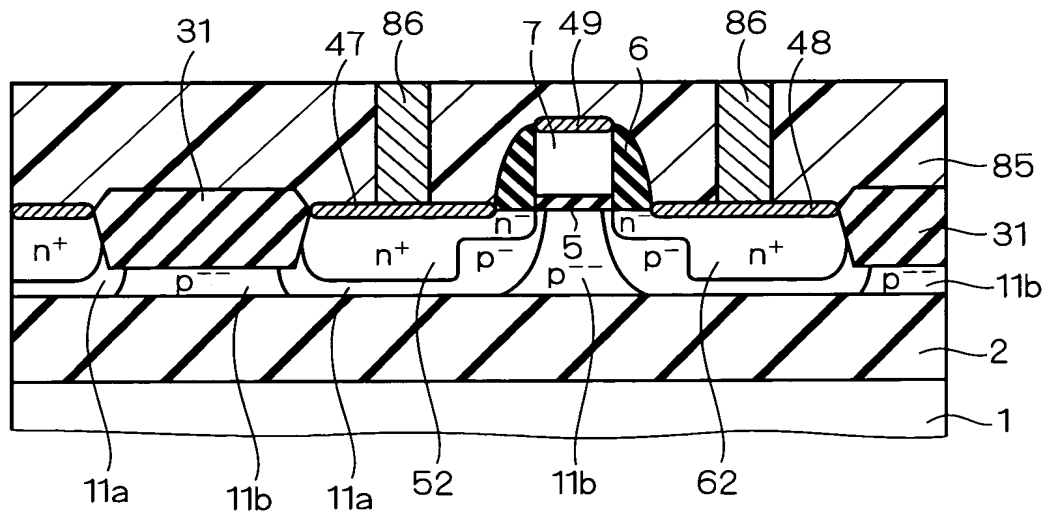


FIG. 51



0995004.1101

FIG. 52

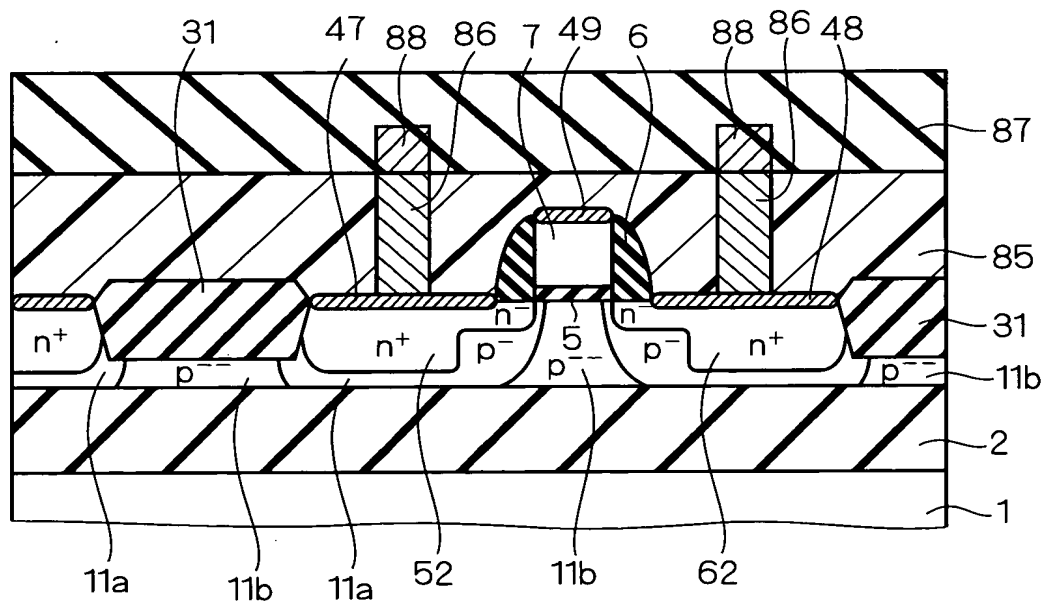
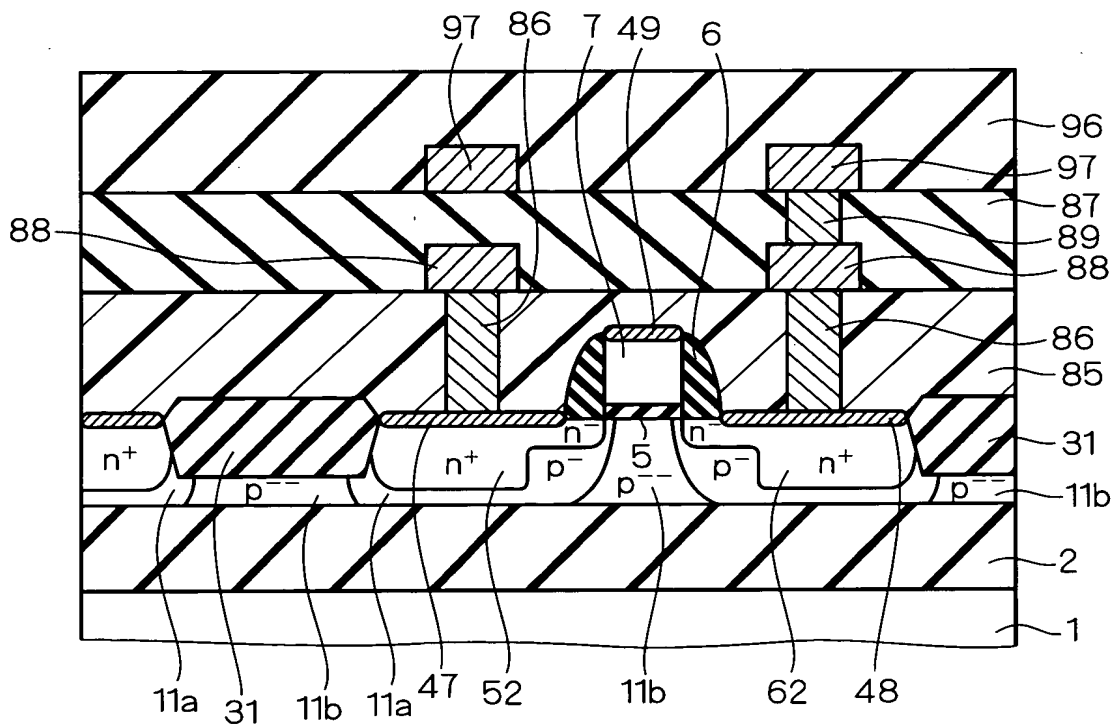


FIG. 53



09986004-110701

FIG. 54

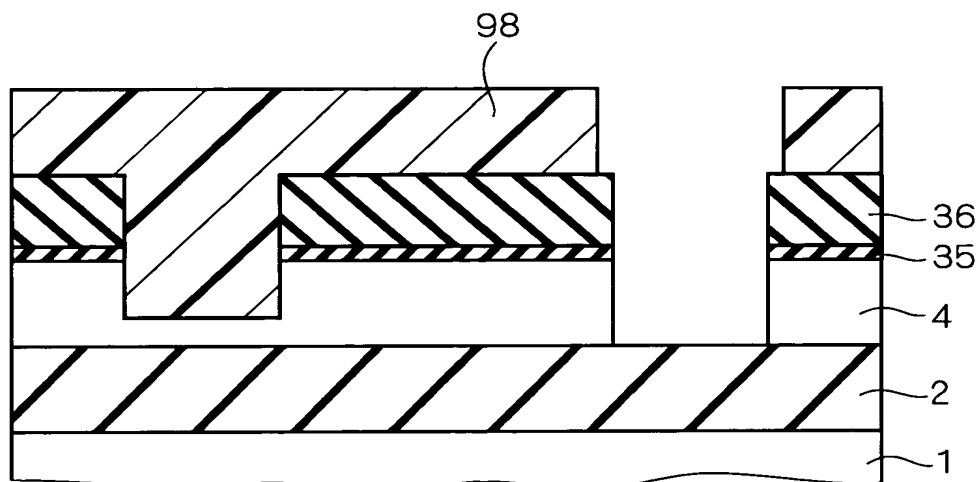
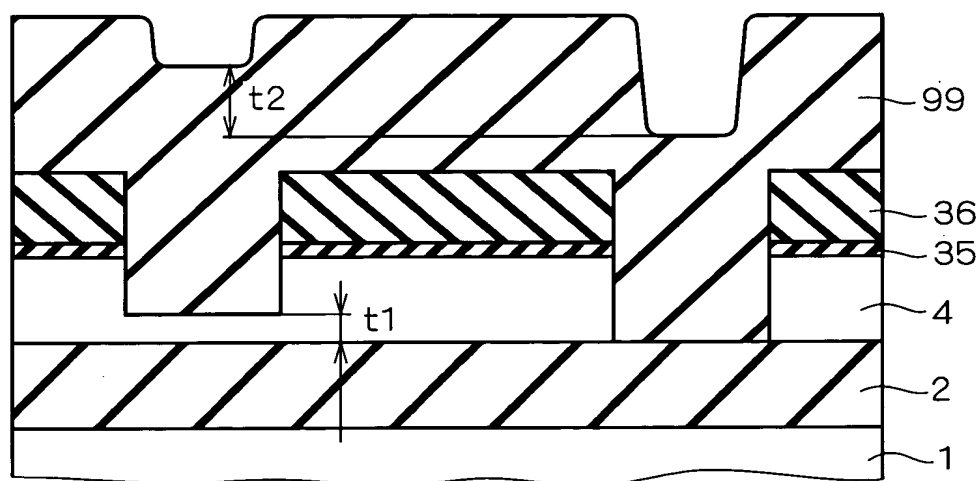


FIG. 55



FOZOTF"40098660

FIG. 56

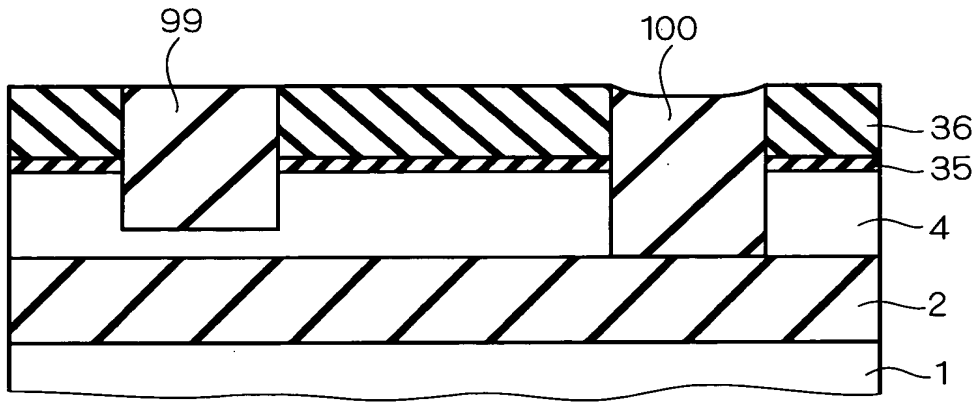
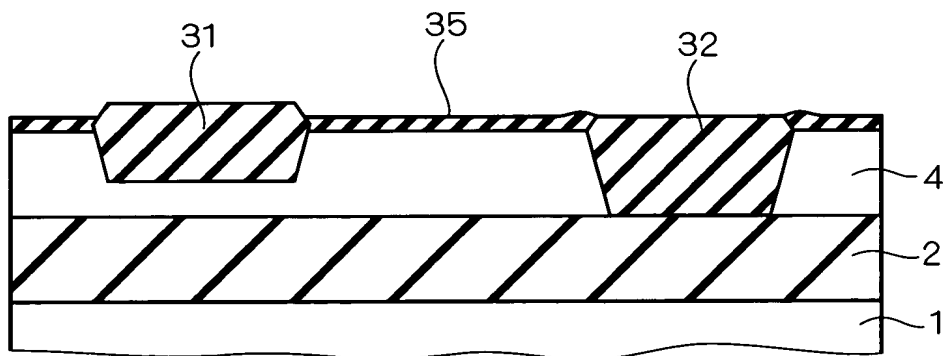


FIG. 57



09986004.110701

FIG. 58

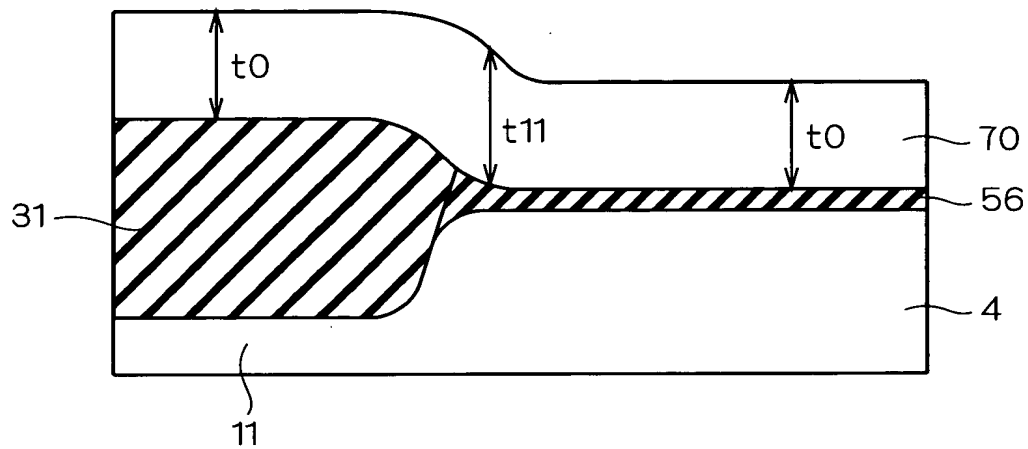
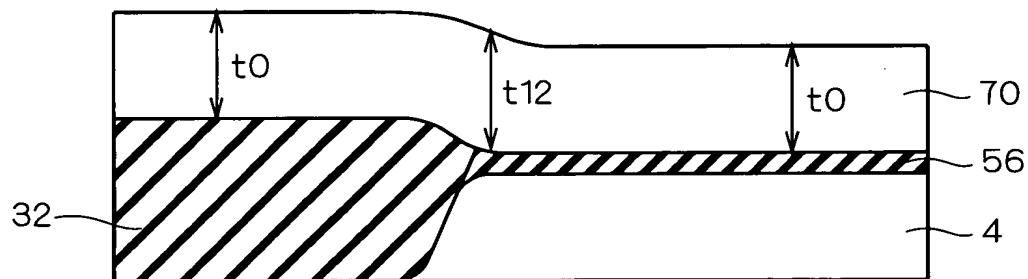


FIG. 59



09986004-110701